# Reduction of Glitch Energy in Binary Weighted Current Steering DAC: Survey

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**Abstract – VLSI technology is to optimize the any type of digital architecture used to enhance the various applications. One of the mainobjectives is to reduce the glitch energy in various systems. The survey is to optimize glitch energy. Different techniques are used to improve the performance by reducing the glitch. Some of the parameters areSpurious Free Dynamic Range (SFDR), Along with Integral Non Linearity (INL), and Differential Non Linearity (DNL) should be analyzed. In which Digital to analog converter (DAC) is used in many applications to convert digital signal to analog signal. The input of the DAC produces some transitions at the output. The transitions areneeded to be reduced by using several techniques. Those techniques helps to reduce the glitch and it improve SFDR and to reduce INL, DNLvalues.Itimprovesthe performance of the system.**

**Index Terms – Glitch energy, binary weighted digital to analog converter (DAC), current switch.**

## 1. INTRODUCTION

Over the last two decades, the CMOS design process has been confronted by a number of seemingly unbeatable technological objections (e.g., the memory wall and the wire delay problem). At each turn, new types of systems have been designed to meet these objections, and microprocessor interpretation has continued to scale with exponentially increasing transistor cost. One or more than two billion transistors integrated on a single chip, power dissipation has become the current critical challenge facing modern die design. The traditional cooling technologies exhaust the maximum On-chip power dissipation. Any further increases will require expensive and objection solutions (e.g., liquid cooling), which should significantly increase overall system cost. Multicore architectures appeared in the early 2000s as a means of neglecting the power wall, increasing similarity under a constant clock frequency to neglect raise in dynamic power consumption. Although multicore systems dose manage to keep power dissipation at day for the past decade, with the approaching transition to 32nm CMOS, they were starting to experience scalability problems of their own. To preserve constant dynamic power at an addicted clock rate, supply and threshold voltages must be scaled with feature size, but this method induces an exponential growth in leakage power, which is fast increase in dynamic power in magnitude. Under thislow scaling behavior, the number of active cores on a chip will had to grow much more slowly than the total transistor cost allows; indeed, at 11nm, over 80% of all cores may have to be latent at all times to fit within the chip's thermal envelope.In applications like wireless transmission, digital video and audio will requires cost-effective data converters that can attain higher speed or conversion rate and resolution. An ample range of digital-to-analog converter (DAC) exists; each has its own merits. The DAC's were classified as R2R LadderDAC;binary weighted DAC Segmented DAC along with Current-steering DAC. Binary weighted DAC, R2R ladder DAC, Segmented DAChas some disadvantagesofmoderateconversion rate. The current-steering DACs can obtain high conversion rate and thus were used in high frequency signals. This type is referred as current-steering DAC since it uses current throughout the conversion has been compared to other DACs where a voltage is transferred into current which is then used to form a voltage at the output.

Current-steering type of DACs needed precision current sources that were summed in various fashions. Current-steering DACs have advantageof high current will drive inherent in the system and, since output buffers were not required to run resistive load this DACs were used in high speed applications. Current steering DACswere classified as two types. First type needs a set of current sources here each of unit value of currentI, i.e. for Nbit 2N-1 current sources are required. Second type is referred as current-steering DAC in additional with binary weighted current sources, as the name specifies current sources were binary weighted and for *N*-bit *N* current sources of different sizes are needed. The one type of current-steering digital to analog converterneeds digital input in the form of thermometer code, on the other hand in another type current-sources were binary weighted thus input code could be a simple binary number. In thermometer code there would be all ones from Least Significant Bit (LSB) to the *j*th bit for digital input *Mj* and all other bits above it are zero. It is named as

thermometer code since code will changes from exclusive once to all zero resembling to thermometer. Current-steering digital-to-analog converters (DACs) perform an important role in communication and video systems. Current-steering DACs have the advantages of speed, linearity, and power efficiency. There are three different architectures to implement the switched current source array, binary, unary, and segmented.

Accounting for power consumption, die size, and complexity, the binary weighted architecture was still a goodcandidate for medium-to-high-resolution and sampling rate. It attains both static and dynamic specifications at low cost. The design approach proposed in this brief can be applied to the LSB part for segmented DACs as well. Glitch is an important measuring parameter in the output signal quality. When the binary-weighted current-steering DAC could operate at a high sampling rate, glitch produced by the transitions of current switches should have significant impact on the derived signal. In the DACs are used in video display systems, excessive glitch can producecolor shifts at the borders of objects results in sparkles on the screen. And also, the spurious free dynamic range (SFDR) was used to quickly reduce with the increasing amplitude of the glitches. It was quickly reduced with the increased amplitude of the glitches. The largest glitch was usually generated during major code transitions, because all of the bits wereswitched and timing skews are exists among different current switches. The glitch energy is defined as whenever the signal converted from digital to analog some transitions are occur. It also consumes some power.So it is necessary to reduce a glitch.

[1] Paper studies the effect of segmentation on current- steering digital-to-analog converters (DACs). Segmentation helpsto improve the dynamic behavior of the converter. Reducing the segmentation degree some methods is given. The presented chip, was carried out of 10-bit binary-weighted current-steering DAC, which has >60 dB SFDR at 250 MS/sfrom DC to Nyquist. At the 62.5 MHz signal frequency and 250 MS/s, operating the device in 9-bit unary, 1-bit binary-weighted mode.

Which obtained 60 dB SFDR in this measurement determines that the nature of theconverter did not limit the SFDRvalue?The chip is draw 4 mW from a dual 1.5 V/1.8 V supply plus load currents. The active area is less than 0.35 $mm^2$in a standard 1P-5M 0.18-µm 1.8-V CMOS process. Both INL and DNL are below 0.1 LSB.Dynamic power is proportional to the square of supply voltage, leads to reducing the voltage significantly reduces dependence on temperature.

[2]Proposed 10bits,500M segmented current steering Digital to Analog converter is designed. The DAC was implemented by using 90nm technology with a supply voltage of 1.2V.The design was implemented with the matching network, which needs for the current sources. Segmented architecture of the DAC was used in order to decrease the glitch and to improve the Monotonicity, even though that increases the cost.

Here the signal to noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) value of the segmented DAC architecture was also analyzed. Monotonicity is guaranteed by using segmented kind of architecture.SFDR and SNDR values are high. Thermometer coded DAC requires large area and power consumption.

[3] Presented a high-speed, low-glitch, and low-power design for a 10-bit binary-weighted current-steering digital-to-analog converter (DAC).Large input buffers are replaced by variable-delay buffers with a compact layout to drive a lot of current switches and re-timing latches. The proposed design to reduce glitch energy from 132 to 1.36 pV s during major code transitions. The calculated spurious free dynamic range (SFDR) has been improved above 10 dB, as compared to DACs without variable-delay buffers. At 250 MS/s update rate, the proposed DAC attains 56 dB SFDR for 0.67 MHz output frequency and 49 dB SFDR for 94 MHz output frequency with 50Ω termination. For static performance, the measuredintegral nonlinearity (INL) and differential nonlinearity (DNL) is belowthe 1.6 and 1.8 LSB, respectively. The proposed DAC can be used in manyapplicationssuch as industry, includingdigital video, digital TV wireless communication system, etc. This chip was implemented in TSMC 1P6M 0.18 µm CMOS technology and dissipates 19mW from a single 1.8 V power supply. The glitch energy is reduced during major code transitioning and DNL values are low. Settling time is increased and Low Monotonicity.

[4]Proposed new techniques of a segmented current steering (CS) digital-to-analog converter (DAC) with also having current sources. The DAC was designed in 0.18 µm CMOS n-well technology provided by National Semiconductor. The 10-bit DAC is fragmented as 5+5, where the 5-LSB bits are executed in double and the 5-MSB bits are actualized in unary design.The overall linearity of the DAC was determined by the matching of unit current sources. Static linearity of the DAC can be expanded by bigger zone of the present source transistors, yielding the element performances. Static linearity of the DAC can be expanded by bigger range of the present source transistors, giving up the dynamic exhibitions. At high recurrence the otherworldly execution of the DAC corrupts due to the expanded parasitic. To achieve improved static as well as dynamic performances here current sources are designed with optimum sizes.In recreation, the DAC gets a most extreme DNL of 0.248 LSB and a greatest INL of 0.440 LSB. The DAC accomplishes a most extreme spurious free element extend (SFDR) of 59.79 dB for 5.37 MHz motion in confound environment at 500MSPS examining rate.The DAC devours just 17.85 mW of force for Nyquist motion at 500 MSPS testing rate with 1.8V supply. It achieves a maximum mismatch simulated SFDR.It achieves improved static and dynamic

performances.It does not consume OFF-state leakage current and support ultra-low power operation.

[5]For high-accuracy current-steering digital-to analog converters (DACs), the delay differences is a major problem which occurs between the current sources. This causes a bad dynamic performance. In this paper, a mathematical model used to deals the effect of the delay differences on the DACs. SFDR property also analyzed.The outcomes are confirmed by correlation with behavioral-level reproductions and to genuine estimation information from distributed papers. According to result analysis, the delay differences cancellation (DDC) technique to reduce the effect of the delay differences on the SFDR property was proposed and verified by simulation results.This method makes utilization of the flexibility in picking the exchanging succession of the switch-and-lock cells, and can enhance the SFDR enormously. The DACs SFDR execution is near that of a perfect DAC which has no defer contrasts. In this architecture the Sleep Control signal transition to low disconnects the FF from ground.

[6]In this paper Proposed Conventional binary-weighted current-steering DACs. These are generally performed with current groups.Where every gathering had a parallel weighted and framed unit current-source exhibits. Dynamic-element matching (DEM) has been performed efficiently with a help of random rotation-based binary-weighted selection (RRBS). Thusperform randomly rotates the sequence of these units to form a new binary-weighted current groups for each DAC outputs. Without utilizing double to-thermometer decoders, RRBS highlights its effortlessness and conservativeness of DEM acknowledgment.RRBS DACs are inhumane to the confuse of little size current-sources and display better element execution contrasted with traditional parallel weighted DAC'S.A 10-bit RRBS DAC is implemented with only 0.034mm2 in a standard 1P6M 1.8V 0.18μm CMOS process. Measured performance attains >61dB spurious-free dynamic range (SFDR) in the Nyquist bandwidth with 500MS/s. To provide better results the proposed RRBS implemented the smallest area for high-speed current-steering DACs up to now. SFDR alsocomparedto 12-bit published designs. Three prevalent figures-of-legitimacy (FOMs) are utilized to contrast this plan and other cutting edge 10~12-piece DACs, with the proposed outline performing best with 2 FOMs. New memory-in-rationale CMOS circuits that can beat various bottlenecks in the current coordinated circuit design. It is not sufficiently high to serenely incorporate with gigabit semiconductor hardware.

[7]Massmarket communication devices such as cable modems and digital set-top boxes the main issue is a cost.In order to reduce needan embedded high-speed high-resolution digital-to-Analog converters (DACs). Here some of architecture is discussed about current- steering digital-to-Analog converter. The main advantages of choosing binary-weighted architecture are consumes less power, required area is low, complexity is low in comparison of other architectures. 14-bit Current steering DAC is implemented and performance parameters are checked. It increase a number of control signals.

[8]The proposed work deals with 12-bit Nyquist current-steering CMOS digital-to-analog converter (DAC).This is a necessary block in baseband section of wireless transmitters. An active analog reconstruction filter is removed in a proposed system using an over sampling (OSR). The optimum segmentation (75%) has been used to produce the better DNL and reduce glitch energy. Monotonicity is guaranteed by this segmentation ratio. Using a new 3-D thermometer decoding method higher performance is achieved which reduces the area, power consumption and the number of control signals of the digital section. Here two digital channels in parallel which leads to reach a 1-GSample/s frequency. Simulation results show that the spurious free-dynamic-range in Nyquist rate is better than 64 dB. Digital part of the chip operates with only 2.4 V but the analog voltage supply is 3.3V. Total power consumption is 144.9 mW. The chip had been processed in a standard 0.35 μmCMOS technology. Active area of chip is 1.37 $mm^2$. Itreduces power consumption and number of control signals. Here using an individual power supplies are used for digital and analog parts. This leads to increase area.

[9]Proposed a Steep-slope hetero-junction tunnel field-effect transistor (HTFET) devices provide a new chance over CMOS in less power high-performance applications. In this paper, optimization is carried 14-bit 1-GS/s current-steering digital-to-analog converter (DAC) using 0.4/0.3 V mixed-supply HTFETs is examined. Device characteristics comparison and circuit analysis this paper presents a HTFET endorses significant differences in both I–Vand C–Vdue to the steepslope tunneling mechanism and a nature of vertically fabricated structure are made. While such differences are significantly affect the circuit design corners. This paper gives the co-optimization of circuit and device for the HTFET DAC.Which reaching at higher current source output impedance, less glitch,and thus provide a better performance over the Si-CMOS DAC.Device variation of HTFET is also discussed here, and static matching accuracyis done by calibration techniques. It is used in low power high performance communication applications. It is also used in low power wideband transceiver. It cannot be used in deep submicron ICs.

[10]Proposed a CMOS 8-bit binary type current steering Digital to Analog Converter DAC. Dynamic random returnto zero technique is used to improve dynamic performance. Advantages of current steering DAC areconstant output impedance and high conversion rate. To establish the proposed technique, 8 bit CMOS DAC was designed and layout is applied in 90 nm technology. Here also analysis the Computation of Integral Nonlinearity (INL) and Differential Non Linearity (DNL) performance parameter. 57 mW powers

were consumed by a chip layout.The area utilization is 5483 $(\mu m)^2$ area. It consumes less power and small overhead in digital circuits. It would not enable power reduction if they were to replace SRAM-based memories. So that the efficiency of the system get improved and speed get increased moderately.

## 2. CONCLUSION

In this survey, the CMOS design of different bit DAC architectures is proposed. In this they reduceglitch energy and improvespurious free dynamic range (SFDR)by using different techniques depends on the applications. There are some limitations to achieve better performance of the system. The major limitations are circuit complexity, rising power, speed and various constrains such as signal to noise ratio and power consumption. My work is to overcome these limitations by proposing new technique Dynamic Compensation Capacitance in DAC. This helps to improve the performance of the DAC by reducing the glitch energy.

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